MOTOROLA

MEX68DB2(D2)

MEX68DB2
DEBUG II MODULE

User's Guide

MICROSYSTEMS

MEX68DB2(D2)
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MEX68DB2
DEbug II Module

User's Guide

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, preparation for use and installation instructions, programming considerations, and theory of operation for the MEX68DB2 DEbug II Module. A typical module is illustrated in Figure 1-1.

1.2 FEATURES

The features of the DEbug II Module include:

- Hardware and firmware that provide most of the system development features of the system.
- Contains the communications interface for user's specific terminal selection.
- Contains EXbug firmware.
- Switch control of dual memory maps and halt-on-address function.
- Jumper selectable baud rate.
- Series II DSB (Dynamic System Bus) provides Page Enable and Parity Error control.
- Bus drive capability.

1.3 SPECIFICATIONS

DEbug II Module specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The DEbug II Module provides the system with the capability of evaluating and debugging the user's prototype system hardware and software. The ROM memory contains the EXbug firmware that provides the system with its unique system development capabilities. The RAM memory acts as a scratch pad memory to the EXbug program. Additional circuitry interfaces the module to the user's terminal, the front panel controls and indicators, and to the system bus. The required hardware to support all the debug capabilities provided in EXbug is also resident on the module.

Three switches are provided on the module for user control of the Map mode, Halt-on-Address, and Restart map.

The Dynamic System Bus (DSB) provides a unified approach for system designers to incorporate system modules into more sophisticated end products. Parity error and page enable lines are connected to the DSB.

An arrangement of pins is provided on the module for the user to jumper select the baud rate of the terminal.

TABLE 1-1. DEbug II Module Specifications

CHARACTERISTIC	SPECIFICATION
Memory Type	
RAM	MOS Static RAM (two 128 x 8 bits)
ROM (Firmware)	Bipolar Static ROM (1024 x 8-bit alterable)
ROM (Firmware)	Bipolar Static ROM (2048 x 8-bit alterable)
Input Signals	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Data Terminal Interface Baud Rate	110, 150, 300, 600, 1200, 2400, 4800, 9600 (jumper selectable)
Operating Temperature	0° to 70°C
Power Requirements	+5 Vdc (1.5 Amps Max.) +12 Vdc (.5 Amps Max.) −12 Vdc (.4 Amps Max.)
Dimensions	
Width and Height	9.75 inches x 6.15 inches
Board Thickness	0.062 inches

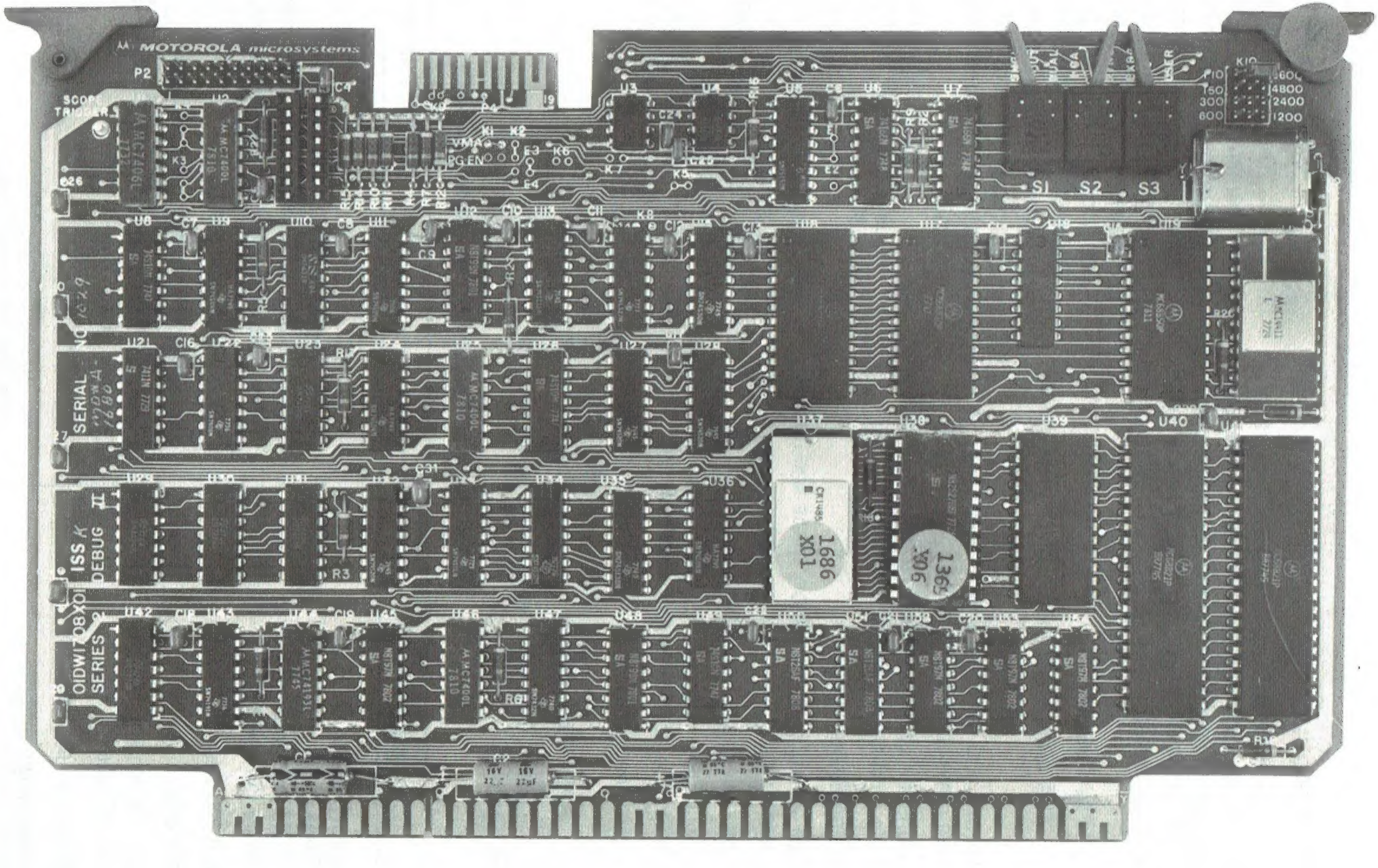


FIGURE 1-1. Typical DEbug II Module

CHAPTER 2
INSTALLATION INSTRUCTIONS, HARDWARE PREPARATION, AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and preparation for use instructions for the MEX68DB2 DEbug II Module. Also included in this chapter are the module interconnection signals and the function of the switches.

2.2 UNPACKING

Unpack the DEbug II Module from the shipping carton and, referring to the packing list, verify that all of the items are present. Save the packing materials for storing and reshipping the module. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

The DEbug II Module should be inspected upon receipt for broken, damaged, or missing parts, and physical damage to the printed circuit board.

2.4 HARDWARE PREPARATION

The DE bug II Module contains the hardware and firmware that provide most of the systems development features of the system. This module contains the communications interface that must be configured for the user's specific terminal selection. Switches that control the use of the dual memory maps and the halt-on-address function are found on this module. Finally, the EXbug firmware is mounted on this module. EXbug has been designed to permit the user to exchange a 1K ROM with a PROM containing user-developed I/O and utility routines. Substitution of firmware is not required for most system applications.

Figure 2-1 illustrates the locations of the user options on the DEbug II Module.

2.4.1 Terminal Interface Options

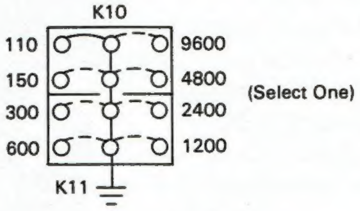
A complete discussion on how to select either a 20 mA interface or an RS-232C interface is presented in the appropriate appendix of the system user's guide. Connector P4 on the module is keyed for proper alignment of the RS-232C terminal interconnect cable or the Micromodule 11 cable. Several jumpers must be installed and circuit track must be cut, depending upon what specific terminal configuration is desired. These are:

K5 — Is factory installed and provides the CLEAR-TO-SEND signal for the RS-232C configuration. It must be removed for 20 mA interfacing.

K6, K7, K8 — Should be installed to apply power to Micromodule 11 when using 20 mA interface. The jumpers are omitted as a precaution against having power active on connector P4.

K9 — Is factory installed for RS-232C interface. It may be removed in those special cases where the data terminal ground is *not* to be connected to the system ground.

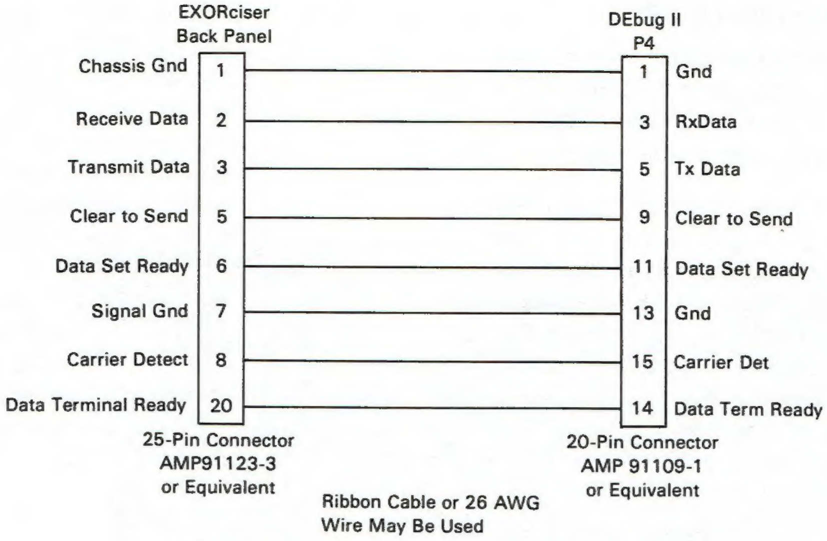
K10, K11 — This 3 x 4 arrangement of jumper pins is used to select the terminal baud rate. This selection is required and identical for both the 20 mA and the RS-232C connections. A plug-in jumper is provided. The jumper selection is illustrated below:



Connector P4, pin 7 — This line, REQUEST TO SEND, is used only when the Micromodule 11 is installed in the system. When the system is used with a Micromodule 11, a jumper must be installed between U3 pin 7 and P4 pin 7. On later versions of this module, the jumper must be installed between E5 and E6. This jumper provides software selectable Reader Control with Micromodule 11.

2.4.2 Transmit/Receive Lines (P4)

In some modems the transmit and receive lines are reversed. Jumper points E1, E2, E3, and E4 are provided so the user may reverse these lines on the module. To do this, the circuit track between E1 and E2, and E3 and E4 must be cut. Jumpers must then be installed between E1 and E4, and E2 and E3. This reverses the transmit and receive lines on connector P4, pins 5 and 3.


EXORciser Back Panel
DEbug II P4
Chassis Gnd 1 — 1 Gnd
Receive Data 2 — 3 RxData
Transmit Data 3 — 5 Tx Data
Clear to Send 5 — 9 Clear to Send
Data Set Ready 6 — 11 Data Set Ready
Signal Gnd 7 — 13 Gnd
Carrier Detect 8 — 15 Carrier Det
Data Terminal Ready 20 — 14 Data Term Ready
25-Pin Connector AMP91123-3 or Equivalent
20-Pin Connector AMP 91109-1 or Equivalent
Ribbon Cable or 26 AWG Wire May Be Used

NOTE: All other pins are unused and should not be connected.

FIGURE 2-2. Interconnect Cable Details

2.5 TERMINAL INTERCONNECT

The DEbug II Module may be installed in an EXORciser I/IA. When this is done, a terminal interconnect cable interfaces an RS-232C terminal with connector P4 on the DEbug II Module. Installation instructions are presented in paragraph 2.6.2. This cable may be purchased from Motorola or fabricated by the user. The Motorola part number is 30BW1635X01. Construction details are shown in Figure 2-2. Signal information is listed in Table 2-4.

2.6 INSTALLATION INSTRUCTIONS

2.6.1 EXORciser II Installation Procedure

Install the DEbug II Module as follows:

(a) Turn power OFF on equipment in which module is being installed.

CAUTION

INSERTING MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON MODULE.

(b) Locate ribbon cable which connects to the front panel RESTART and ABORT switches, and the VUA and VXA indicators. This ribbon cable with 16-pin DIP connector approaches the card cage from the rear of the chassis. Connect this cable to connector P3 on the DEbug II Module.

(c) Install module in selected card slot. This module may be installed in any of the card slots in the system.

(d) Locate ribbon cable which connects to the rear panel RS-232C connector. This ribbon cable, with a 20-pin edge connector, approaches the card cage from the rear of the chassis. Connect this cable to connector P4 on the DEbug II Module. Connect the RS-232C type terminal to the rear panel connector.

NOTE

If Micromodule 11 is installed, connect ribbon cable from Micromodule 11 to connector P4 on DEbug II Module. RS-232C cable is not used in this case.

(e) Turn power ON.

2.6.2 EXORciser I/IA Installation Procedure

Install the DEbug II Module as follows:

(a) Turn power OFF on equipment in which module is being installed.

CAUTION

INSERTING MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON MODULE.

(b) The Baud Rate Module is located on the inside of the rear panel. Locate the ribbon cable that connects the front panel RESTART and ABORT switches and indicators to the Baud Rate Module. Disconnect this cable from the Baud Rate Module and connect to P3 on the DEbug II Module.

(c) Install the module in selected card slot. This module may be installed in any of the card slots in the system.

(d) Four mounting brackets are provided on the top edge of the chassis rear panel. Install the 25-pin connector of the terminal interconnect cable (paragraph 2.5) under one of these brackets. This connector should face the rear of the chassis. Connect the 20-pin connector to P4 on the DEbug II Module. Connect the RS-232C type terminal to this rear panel connector.

NOTE

If Micromodule 11 is installed, disregard step 'd' above, and connect Micromodule 11 cable to P4 on DEbug II Module.

(e) Turn power ON.

2.7 USING DEbug II WITH SERIES I MPU MODULE

The series II MPU Module MEX6800-2 generates a Three-State Grant (TSG) signal as an acknowledgement that the TSC signal has been recognized. The Series II DEbug II Module interfaces with this TSG signal, whereas the Series I DEbug Module interfaces directly to a user generated TSC signal. In order to interface a DEbug Module with a Series I MPU Module, the TSG line on the system bus must be grounded. This is pin 15 on the system bus. In this case, TSC may not be used with this configuration.

2.8 MODULE INTERCONNECTIONS

The DEbug II Module interconnects directly with the system bus. Table 2-1 lists each pin connection, signal mnemonic, and signal characteristic. Table 2-2 identifies the Dynamic System Bus interface signals on connector P2. Table 2-3 identifies the interface signals on connector P3. Table 2-4 identifies the signals on the terminal interface connector P4.

TABLE 2-1. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
A,B,C	+5 Vdc	+5 Vdc Power / Used by the module logic circuits.
D	$\overline{\text{IRQ}}$	INTERRUPT REQUEST — A low level sensitive input signal used to request generation of an interrupt sequence. The instruction being executed will be completed before the request is recognized.
E	$\overline{\text{NMI}}$	NON-MASKABLE INTERRUPT — A low going, edge sensitive output signal to the MPU II Module used to request generation of an MPU non-maskable interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, regardless of the logic state of the Interrupt Mask bit in the MPU Condition Code Register, the MPU will begin executing the non-maskable interrupt.
F	VMA	VALID MEMORY ADDRESS — A high level, TTL compatible signal produced by the MPU II Module and used to indicate to the DEbug II Module that a valid memory address is present on the address bus.
H		Not Used
J	$\phi 2$	Phase 2 — One of the bi-phase clock signals generated by the clock circuit on the MPU II Module.
K,L		Not Used
M	−12 Vdc	−12 Vdc Power — Used by the module logic circuits.
N		Not Used
P	BA	BUS AVAILABLE — A normally low level input signal from the MPU II Module that, when activated, goes high to indicate that the MPU has halted and the address bus is available. This condition occurs whenever the GO/HALT signal is in the HALT (low) state or the MPU is in the WAIT state as a result of executing a Wait instruction. When this occurs, all of the MPU three-state output drivers will go to their off (high impedance) state and other outputs to their normally inactive state. A maskable interrupt or non-maskable interrupt removes the MPU from the WAIT state.
R,S		Not Used
T	+12 Vdc	+12 Vdc Power — Used by the module logic circuits.
U,V		Not Used
W	$\overline{\text{PARITY ERR}}$	PARITY ERROR — This signal line is normally held high by the DEbug II Module. If a memory module that incorporates a parity check circuit is used within the system and a parity error is detected, this signal will be forced low for one clock cycle.

TABLE 2-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
X,Y,Z	GND	GROUND
$\overline{\text{A}}$	$\overline{\text{FIRQ}}$	FAST INTERRUPT REQUEST — When a logic zero is recognized at this output, the MC6809 places only the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{\text{FIRQ}}$ vector location to obtain the starting location of the $\overline{\text{FIRQ}}$ service routine.
$\overline{\text{B}}$,$\overline{\text{C}}$		Not Used
$\overline{\text{D}}$,$\overline{\text{E}}$,$\overline{\text{F}}$		
$\overline{\text{H}}$	$\overline{\text{D3}}$	DATA bus (bit 3) — One of 8 bidirectional data lines used to provide a two-way data transfer between the MPU II Module and all other plug-in modules within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a memory read or write operation.
$\overline{\text{J}}$	$\overline{\text{D7}}$	DATA bus (bit 7) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
$\overline{\text{K}}$	$\overline{\text{D2}}$	DATA bus (bit 2) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
$\overline{\text{L}}$	$\overline{\text{D6}}$	DATA bus (bit 6) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
$\overline{\text{M}}$	A14	ADDRESS bus (bit 14) — One of 16 address lines from the MPU II Module that permits the MPU to select any addressable memory location within the system.
$\overline{\text{N}}$	A13	ADDRESS bus (bit 13) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{P}}$	A10	ADDRESS bus (bit 10) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{R}}$	A9	ADDRESS bus (bit 9) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{S}}$	A6	ADDRESS bus (bit 6) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{T}}$	A5	ADDRESS bus (bit 5) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{U}}$	A2	ADDRESS bus (bit 2) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{V}}$	A1	ADDRESS bus (bit 1) — Same as A14 on Pin $\overline{\text{M}}$.
$\overline{\text{W}}$,$\overline{\text{X}}$,$\overline{\text{Y}}$	GND	GROUND
1,2,3	+5 Vdc	+5 Vdc Power — Used by the module logic circuits.
4	$\overline{\text{HALT}}$	HALT — This low level input is level sensitive. Indicates to the DEbug II that the MPU is in the HALT mode. In this mode, the MPU will stop at the end of an instruction, the BUS AVAILABLE signal will go high, the VALID MEMORY ADDRESS signal will go low, and all other three-state lines will be changed to their off or high impedance state.
5	$\overline{\text{RESET}}$	RESET — This buffered input/output signal to/from the MPU II Module is used to restart the system when power is initially applied. Restart occurs on the low-to-high transition of the RESTART signal. If the RESTART pushbutton switch, located on the front panel of the system, is depressed while the system is operating, the low-to-high transition of the RESET signal will cause the MPU II Module to execute the EXbug restart routine or the restart routine indicated by the user.
6	R/$\overline{\text{W}}$	READ/WRITE — This signal is generated by the MPU II Module and indicates to the other modules contained within the system that the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Additionally, when the MPU is halted, this signal will be in the read state.

TABLE 2-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
7,8,9		Not Used
10	VUA	VALID USER'S ADDRESS — This signal is produced by the DEbug II Module. When high, this signal indicates that the address on the address bus is valid and the MPU II Module is *NOT* addressing the EXbug Program.
11	−12Vdc	−12 Vdc Power — Used by the module logic circuits.
12,13		Not Used
14	$\overline{\text{DEBUG}}$	DEBUG — This line, connected to ground on the DEbug II Module, indicates to the MPU II Module that the DEbug II Module is installed in the system. This is used to determine whether the VALID USER'S ADDRESS (VUA) signal is controlled by the DEbug II Module or the MPU II Module. When the DEbug II Module is *NOT* used, the MPU II Module forces this signal line high.
15	TSG	THREE-STATE GRANT — This signal is generated by the $\overline{\text{MPU}}$ II Module in response to a THREE-STATE CONTROL request ($\overline{\text{TSC}}$). During normal operation, the TSG signal is low. During a three-state operation, the signal is made high.
16	+12 Vdc	+12 Vdc Power — Used by the module logic circuits.
17,18		Not Used
19	VXA	VALID EXECUTIVE ADDRESS — A high level signal generated by the DEbug II Module in place of the VUA signal (refer to description of VUA on Pin 10) when the system is operating in the Dual Map Mode and the EXbug Program is addressing the Executive portion of the memory map. Additionally, all peripheral modules (such as memories) must be set to respond to the VXA signal if the user wants to operate those modules in the Executive portion of the map.
20,21,22	GND	GROUND
23,24,25		Not Used
26,27,28		
29	$\overline{\text{D1}}$	DATA bus (bit 1) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
30	$\overline{\text{D5}}$	DATA bus (bit 5) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
31	$\overline{\text{D0}}$	DATA bus (bit 0) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
32	$\overline{\text{D4}}$	DATA bus (bit 4) — Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$.
33	A15	ADDRESS bus (bit 15) — Same as A14 on Pin $\overline{\text{M}}$.
34	A12	ADDRESS bus (bit 12) — Same as A14 on Pin $\overline{\text{M}}$.
35	A11	ADDRESS bus (bit 11) — Same as A14 on Pin $\overline{\text{M}}$.
36	A8	ADDRESS bus (bit 8) — Same as A14 on Pin $\overline{\text{M}}$.
37	A7	ADDRESS bus (bit 7) — Same as A14 on Pin $\overline{\text{M}}$.
38	A4	ADDRESS bus (bit 4) — Same as A14 on Pin $\overline{\text{M}}$.
39	A3	ADDRESS bus (bit 3) — Same as A14 on Pin $\overline{\text{M}}$.
40	A0	ADDRESS bus (bit 0) — Same as A14 on Pin $\overline{\text{M}}$.
41,42,43	GND	GROUND

TABLE 2-2. Connector P2 Dynamic System Bus

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
17	$\overline{\text{PARITY-ERR}}$	PARITY ERROR — Same as PARITY ERROR ON P1-W. Jumper selectable.
18	GND	GROUND
19	$\overline{\text{PAGE ENA}}$	PAGE ENABLE — If a user builds a controller that can convert the VMA signal from the MPU into one of several pages, an unlimited number of "pages" of 64K bytes can be realized. This signal port is jumper selectable.
20	GND	GROUND

TABLE 2-3. Connector P3 Front Panel Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1		Not Used
2	RUN/VUA	RUN/VALID USER ADDRESS — This high level signal turns on the VUA indicator on the fornt panel when the system is executing in the User Map. If the DEbug II Module is installed in an EXORciser I/IA, this signal turns on the RUN indicator on the fornt panel.
3	AUX/VXA	AUXILIARY/VALID EXECUTIVE ADDRESS — This high level signal turns on the VXA indicator on the front panel when the EXbug Firmware is being executed. If the DEbug II Module is installed in an EXORciser I/IA, this signal turns on the AUX indicator on the front panel.
4		Not Used
5	ABORT NO	ABORT NORMALLY OPEN — Refers to the front panel ABORT momentary contact switch. This line is held high until the ABORT switch is pressed, at which time an NMI (Non-maskable Interrupt) is generated, causing control to be returned to the EXbug routine.
6		Not Used
7	RESTART NC	RESTART NORMALLY CLOSED — Refers to the front panel RESTART mementary contact switch. (See pin 11 for explanation.)
8,9	GND	GROUND
10		Not Used
11	RESTART NO	RESTART NORMALLY OPEN — Refers to the front panel RESTART momentary contact switch. This line is held high until the RESTART switch is pressed, at which time the RESTART signal is supplied to the system to reset all hardware that recognizes Restart. The system initializes itself through the EXbug initialization firmware.
12	ABORT NC	ABORT NORMALLY CLOSED — Refers to the front panel ABORT momentary contact switch. (See pin 5 for explanation.)
13,14		Not Used
15	PWR	POWER — Not connected on the front panel in EXORciser II. When DEbug II Module is installed in EXORciser I/IA, provides low current +5 Vdc to turn on PWR indicator when system is turned on.
16	+5 Vdc	+5 Vdc — Not conncected on the front panel in EXORciser II. When DEbug II Module is installed in EXORciser I/IA, provides +5 Vdc to front panel.

TABLE 2-4. Connector P4 Terminal Interconnect Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	GND	GROUND
2		Not Used
3	RxDATA	RECEIVED DATA — An RS-232C compatible serial data input signal from the terminal, or Micromodule 11 when used.
4		Not Used
5	TxDATA	TRANSMITTED DATA — An RS-232C compatible serial data output signal to the terminal, or Micromodule 11 when used.
6		Not Used
7	REQ TO SND	REQUEST TO SEND — An RS-232C compatible output signal used as a Reader Control to the terminal. This signal is used only with Micromodule 11 (paragraph 2.4.1).
8		Not Used
9	CLEAR TO SEND	CLEAR TO SEND — This output line is a high level when the RS-232C device is ready to receive data.
10		Not Used
11	DATA SET RDY	DATA SET READY — This line is a high level when an RS-232C device is connected and the device is operating.
12		Not Used
13	GND	GROUND
14	DATA TERM RDY	DATA TERMINAL READY — This input line indicates to the RS-232C device that the Basic Display Unit is ready.
15	CARRIER DET	CARRIER DETECT — This output line is a high level when the RS-232C device has detected the carrier signal.
16	+5 Vdc	+5 Vdc — Provides +5 Vdc to Micromodule 11 when used.
17	GND	GROUND
18	−12 Vdc	−12 Vdc — Provides −12 Vdc to Micromodule 11 when used.
19	GND	GROUND
20	+12 Vdc	+12 Vdc — Provides +12 Vdc to Micromodule 11 when used.

CHAPTER 3
PROGRAM OPERATION

3.1 EXbug SUBROUTINES AND ENTRY POINTS

This chapter lists and describes the subroutines in EXbug that are available to run programs. Since EXbug is in the Executive Map, any program that uses EXbug routines must also be in the Executive Map if the system is being operated in the Dual Map Mode. Programs run in the Single Map Mode can also use EXbug routines. Table 3-1 lists the name of the subroutine, the entry point, and the description of the subroutine function.

TABLE 3-1. EXbug Subroutines

MNEMONIC	ENTRY POINT	DESCRIPTION
PWRUP	F000	Enter EXbug from restart. Configure EXbug and its peripherals from a restart or power-up condition. EXbug parameters, as an output, are initialized along with the EXbug peripheral devices. The EXbug startup message is sent to the terminal. NOTE: Control is not returned to the calling program, but is given to the EXbug command input routine.
XBEGEN	F003	Input Start and End addresses. Requests input of beginning and ending address. Verifies inputs are hexadecimal characters. Verifies ending address is larger than beginning address. The output is: $FF0A BEGA 16 Bit Beginning address $FF0C ENDA 16 Bit Ending address NOTE: Acc A and B and the index register are used by this subroutine. If their contents are meaningful, they must be saved prior to calling this subroutine. If single parameters are entered for BEG or END, the default debug offset (Q in locations $FFE1, $FFE2) will be added to them to determine BEGA and ENDA. If two parameters separated by a comma are entered, they will be added together to determine the address being entered. The calling program may modify Q to specify the default debug address. However, if it does this, the new value of Q will be used by EXbug as the default debug offset.
XCBCDH	F006	Convert a hexadecimal character to a binary number. Verifies input is a hexadecimal digit character. Converts character to a 4-bit binary number with HI order 4 bits equal zero. Sets N (negative) condition code for non-hexadecimal characters. Character to convert must be in Acc A. If hexadecimal character input, Acc A contains the 4-bit binary number represented by the input character and the N (negative) condition code is cleared. If non-hexadecimal character input, Acc A contains the character input and the N condition code is set. The B and X registers are preserved.

TABLE 3-1. EXbug Subroutines (cont-d)

MNEMONIC	ENTRY POINT	DESCRIPTION
XCHEXL	F009	Convert most significant binary value to hexadecimal. Converts the most significant 4 bits of Acc A to an ASCII coded hexadecimal character. The B and X registers are preserved.
XCHEXR	F00C	Convert least significant binary value to hexadecimal. Converts the least significant 4 bits of Acc A to an ASCII coded hexadecimal digit character. The A and B registers are preserved.
XINADD	F00F	Input a hexadecimal address. Converts up to 4 input hexadecimal characters to a 16-bit binary address. Index register contains address to store result. Most significant 8 bits of resultant 16-bit address will be stored in the memory location specified by the index register. The least significant 8 bits will be stored in the next higher memory location. Acc A will contain last character input. Acc B will contain number of input hexadecimal characters. Index register is unchanged. The subroutine returns to the calling program when an invalid character or the fifth hexadecimal digit is entered. NOTE: This address is not modified by the default debug offset.
XINCH	F012	Input one character. Waits for and accepts input of one character from debug terminal and echoes back to terminal, if required. There is a no echo flag (AECHO) at $FF53. It must be set non-zero before each call to XINCH for each character that is not to be echoed to the terminal (and line printer, if the Z option is on). Acc A contains 8-bit input character as received from the debug terminal. XINCH clears AECHO if it was non-zero. The B and X registers are preserved.
XINCHN	F015	Input one character with no parity. Waits for and accepts input of one character from debug terminal and echo character back to terminal, if required. Clears HI order bit of input character. There is a no echo flag (AECHO) at $FF53. It must be set non-zero before each call to XINCHN for each character that is not to be echoed to the terminal (and line printer, if the Z option is on). Acc A contains input character as received from debug terminal with the HI order bit cleared. XINCHN clears AECHO if it was non-zero. The B and X registers are preserved.
XOUTCH	F018	Output one character. Outputs one character with required speed fill. Acc A contains character to output to the debug terminal (and to the line printer, if Z option is on). Acc A contains the character output. The B and X registers are preserved.

TABLE 3-1. EXbug Subroutines (cont'd)

MNEMONIC	ENTRY POINT	DESCRIPTION
XOUT2H	F01B	Output two hexadecimal characters and a space. Converts the contents of an 8-bit binary byte to two hexadecimal characters and outputs them followed by a space character to the debug terminal. Index register contains address of the byte to be converted and output. Acc A contains last character output. The index register is incremented by one. The B accumulator is preserved.
XOUT4H	F01E	Output four hexadecimal characters and a space. Converts the contents of two consecutive 8-bit binary bytes to four hexadecimal characters and outputs them followed by a space character to the debug terminal. Index register contains address of the first byte to be converted and output Acc A contains last character output. The index register contains the input address plus 2. The B accumulator is preserved.
XPCRLF	F021	Print CR/LF/Null. Outputs a carriage return, a line feed, and a null character to the debug terminal with required speed fill. Acc A will contain a null character (0). The B and X registers are preserved.
XPDATA	F024	Print CR/LF/Data string. Outputs a carriage return, a line feed and the user specified string of data characters to the debug terminal. Index register will contain the starting address of user data string to output. Output string is terminated by an EOT (04) character. Index register will contain, as an output, the address of the EOT character. Acc A will contain the EOT character. The B accumulator is preserved.
XPDAT1	F027	Print data string. Outputs a user specified string of data characters to the debug terminal. Index register will contain the starting address of user data string to output. Output string is terminated by an EOT (04) character. Index register will contain, as an output, the address of the EOT character. Acc A will contain the EOT character. The B accumulator is preserved.
XPSPAC	F02A	Print space. Outputs a space character to the debug terminal. Acc A will contain, as an output, a space character. The B and X registers are preserved.

CHAPTER 4
THEORY OF OPERATION

4.1 INTRODUCTION

This chapter provides a block diagram description of the MEX68DB2 DEbug II Module. A block diagram of the module is illustrated in Figure 4-2 and the schematic diagram is presented in Figure 4-3.

4.2 BLOCK DIAGRAM DESCRIPTION

As shown in Figure 4-2, the individual blocks in the diagram are connected together with signal lines. Where these lines represent one signal, the signal is named. If several signals interconnect two blocks, the signal name is omitted. An exception to this is the ENABLE signals from the Address Decode. For example, the RAM ENABLE includes RAM Select ($\overline{\text{RAMS}}$), ϕ2, and R/W, while the ROM ENABLE includes 1K Select (1$\overline{\text{KS}}$) and 2K Select (2$\overline{\text{KS}}$).

All addressable elements are ultimately enabled by VXA. VXA is taken from the system bus so that a specially designed user module could address these devices by generating VXA after three-stating VXA from the DEbug II Module.

The majority of signals to/from the system bus are buffered. This protects the circuitry on the module from misapplications at the bus, as well as providing the necessary drive capability where applicable. The data lines are enabled by DATA BUFFER ENABLE (DATA-BUF-EN). This signal enables the data lines as inputs at all times except when a device on the module is being read.

ROM, RAM, Halt-on-Address Detect: The EXbug ROM and RAM addresses are shown in the block diagram and are self-explanatory. The RESTART vector addresses reside in the 2K ROM at all times in order to provide the Executive Restart. The User's Restart vector resides in VUA addressed memory when in the Dual Map Mode.

The Halt-on-Address Detect logic compares A0-A15 from the system bus with the 16 bits stored in PIA1. Since the Halt can be set in the VUA or VXA map, COMPARE VUA (COMP-VUA) from PIA2 defines in which map the halt will occur. The Stop-on-Address Enable (S0A-EN) from PIA1 must also be set before a compare pulse is enabled to the Scope Trigger. If switch S2 is in the HOA (Halt-on-Address) position, a Stop-on-Address NMI (S0A-NMI) occurs and enables the NMI generator circuitry. The EXbug NMI service routine polls to find the cause of the NMI, and CB1 of PIA1 indicates that S0A-NMI is the cause. Since the NMI is recognized by the MPU after execution of the current instruction, if the user sets an op code address into the H0A PIA, EXbug normally halts after that instruction is executed.

ACIA, RS-232C Interface: ACIA and RS-232C Interface control the input/output to the user's terminal that directly interfaces with EXbug. Most of the terminal I/O is software controlled by EXbug. This interface can be modified if the user substitutes his own 1K PROM/ROM at location U38. The only hardware required is buffers to convert the signals to/from RS-232C levels and the generation of the Transmit/Receive CLOCK (TX/RX CLOCK). The user selects the TX/RX CLOCK speed at K10 or K11 (BAUD RATE SELECT).

Front Panel Interface, NMI Generator: The Front Panel Interface Logic interfaces to the indicators and switches on the front panel of the system chassis. The VUA and VXA signals are taken directly from the system bus and buffered so that the LED's will indicate VUA and VXA accurately even if VUA and VXA are driven by specially designed user logic. The RESTART and ABORT debounce logic provides clean signals for the system from the front panel controls. Switch S3 determines whether a USER RESET (USER RST) or an EXBUG RESET (XBUG RST) is generated by the front panel RESTART.

The NMI generation logic can be initiated by four different signals. Three of these signals initiate the NMI circuitry and the fourth modifies the result. NMI is generated by S0A-NMI, ABORT, or Parity Error Acknowledge (PAR-ER-ACK). Parity Error (PAR-ER) is an input to PIA2 and, if the memory parity error interrupt has been enabled via the EXbug " ; ; " command, PIA2 automatically generates PAR-ER-ACK whenever PAR-ER is pulled low.

In the above three cases, the NMI line is pulled low immediately. To assure that the current instruction is completed, the registers preserved, and the MPU is solidly into the NMI service routine, a counter holds NMI low for 32 cycles. The program registers are stored on the stack in the map (VUA or VXA) in which the program was executing. In the Dual Map Mode, the NMI vector must be pulled from the VXA map, if the DEbug II generated the NMI, to assure that EXbug will process it. NMI-ENABLE tells the Force VXA Logic that the NMI was generated by the DEbug II and that the NMI vector must come from the VXA map.

The remaining input to the NMI circuitry is the Run One Instruction (ROI) signal. ROI causes NMI to be pulled low after a delay. In the Dual Map Mode, EXbug first sets up PIA2 to allow an RTI to be executed from the User's map. This restores the user's registers, after which the next instruction is executed. The NMI counter is initiated just before the

RTI is executed by a CA2 from PIA2. It begins counting and the NMI Generator Logic pulls NMI low during the first cycle of the first instruction after RTI. One user instruction is executed, after which the NMI is serviced. NMI is held low for 32 cycles.

In each of the above four cases, a flag is available to the EXbug NMI service routine to determine the origin of the NMI. The IRQ flag in the Control Register of PIA2 is available from a parity error while CA1, CB1, and CB2 of PIA1 indicate ABORT, S0A-NMI, and ROI, respectively.

VUA/VXA Control, Load Logic, Dual Map Shift Register: These three circuits generate the VUA and VXA pulses which provide the system with Dual Map capability. PIA2 provides the software control of this feature. The VUA/VXA Control turns VMA into either VUA or VXA. This is determined by switch S1. If S1 is in the OUT position, VUA duplicates VMA and VXA is low. If S1 is in the SINGLE position, FXXX determines the output. If the address on the bus is within the F000 to FFFF range, VXA duplicates VMA and VUA is held low. For any other address, VUA duplicates VMA and VXA is held low. When S1 is in the DUAL position, both 64K byte maps are accessible. A RESET will force both VUA and VXA low, regardless of S1 position.

To better understand the concept of the Dual Map control logic, the basic elements of the circuitry are shown in Figure 4-1. The output of the shift register, Shift Register VUA (SR-VUA), generates a VUA pulse when high and a VXA pulse when low, depending on VMA.

The shifting and loading of this register are synchronized with ø2, and the flip-flop on CA2 assures that only one load pulse is generated by CA2. PIA2 determines what must be loaded into the shift register. Rather than load all 16 bits plus the shift register input, the applications in EXbug are accomplished with four loadable inputs. The basic operation of the shift register is to load it, and then every ø2 pulse shift the contents up one position. Each time the register shifts, the contents of the serial input flip-flop is loaded into position A of the shift register, and the contents of position S are shifted out of the register.

In order to store a byte in a VUA memory location while EXbug is operating in its VXA memory map, EXbug could use an STAA instruction. Table 4-1 shows a cycle-by-cycle description of the shift register load and shift operation. Prior to executing the code in Table 4-1, EXbug would have loaded the

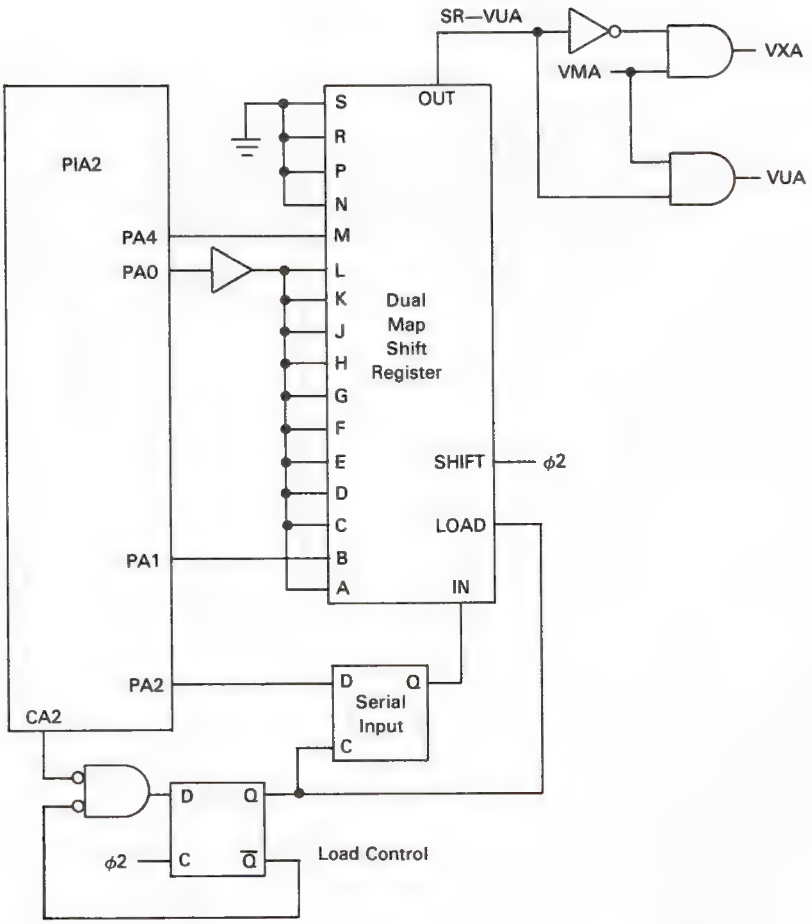


FIGURE 4-1. VUA/VXA Generation Circuitry — Dual Map Mode

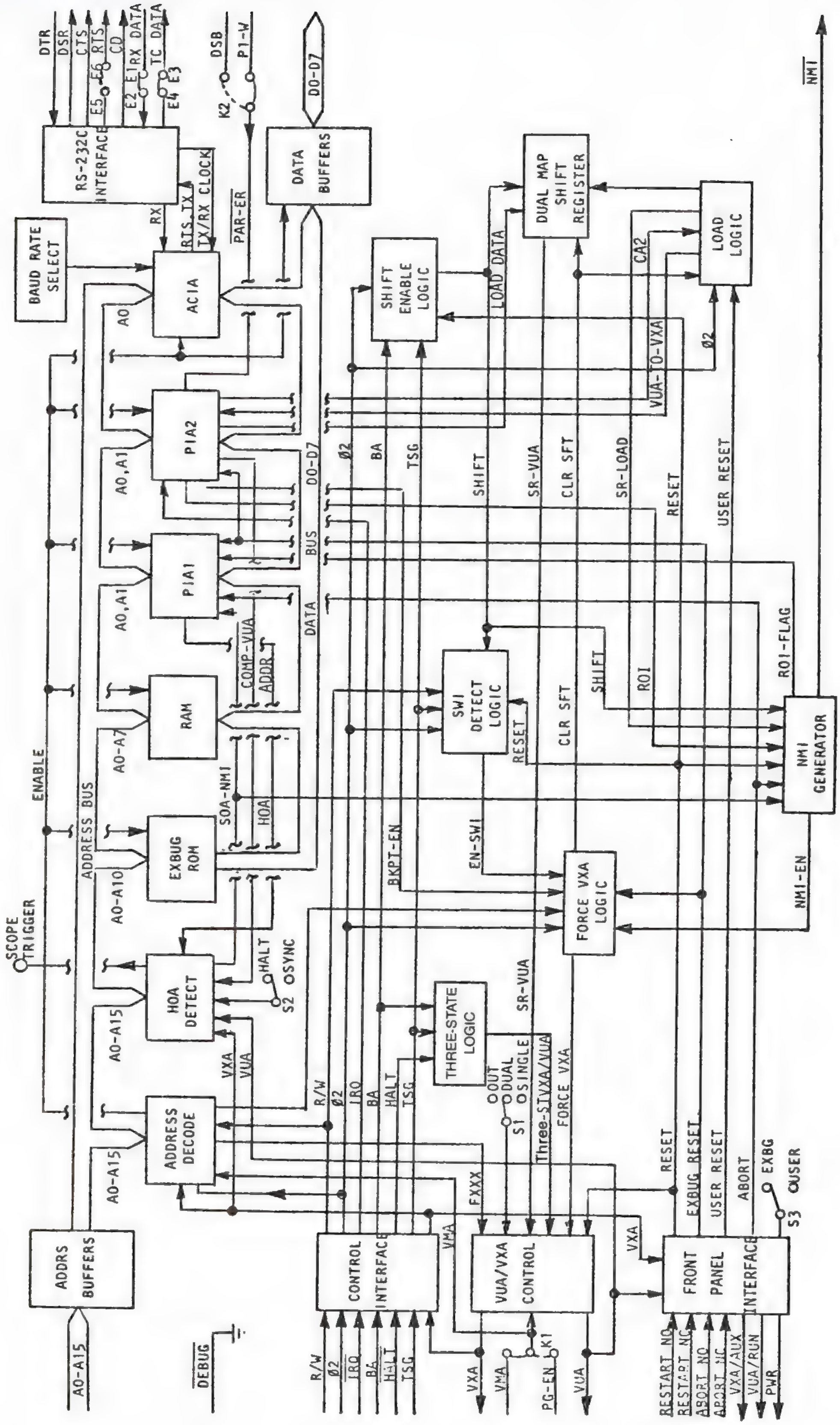


FIGURE 4-2. DEbug II Block Diagram

A Data Register with PA4=1 and PA0=PA1=PA2=0. The data to be stored would have been loaded in Accumulator A, and A Control Register would have been set up to generate a pulse when the A Data Register was accessed. The code in Table 4-1 would then be executed.

The CPX instruction accesses the A Data Register of PIA2, generating a CA2 and, therefore, initiating the load sequence. The CPX instruction was chosen because it accesses the required memory location, generates the load pulse at the correct cycle, and modifies only the Condition Code Register. The actual load occurs in cycle 1 of the STAA. The shifting occurs every cycle after loading so that when the data is actually stored in cycle 6, the output of the shift register is a "1" and the VMA pulse is, therefore, converted to a VUA pulse for this one cycle. After that cycle, the shift register continues shifting, but its "0" output continues to generate VXA pulses so that EXbug is still in control of the execution.

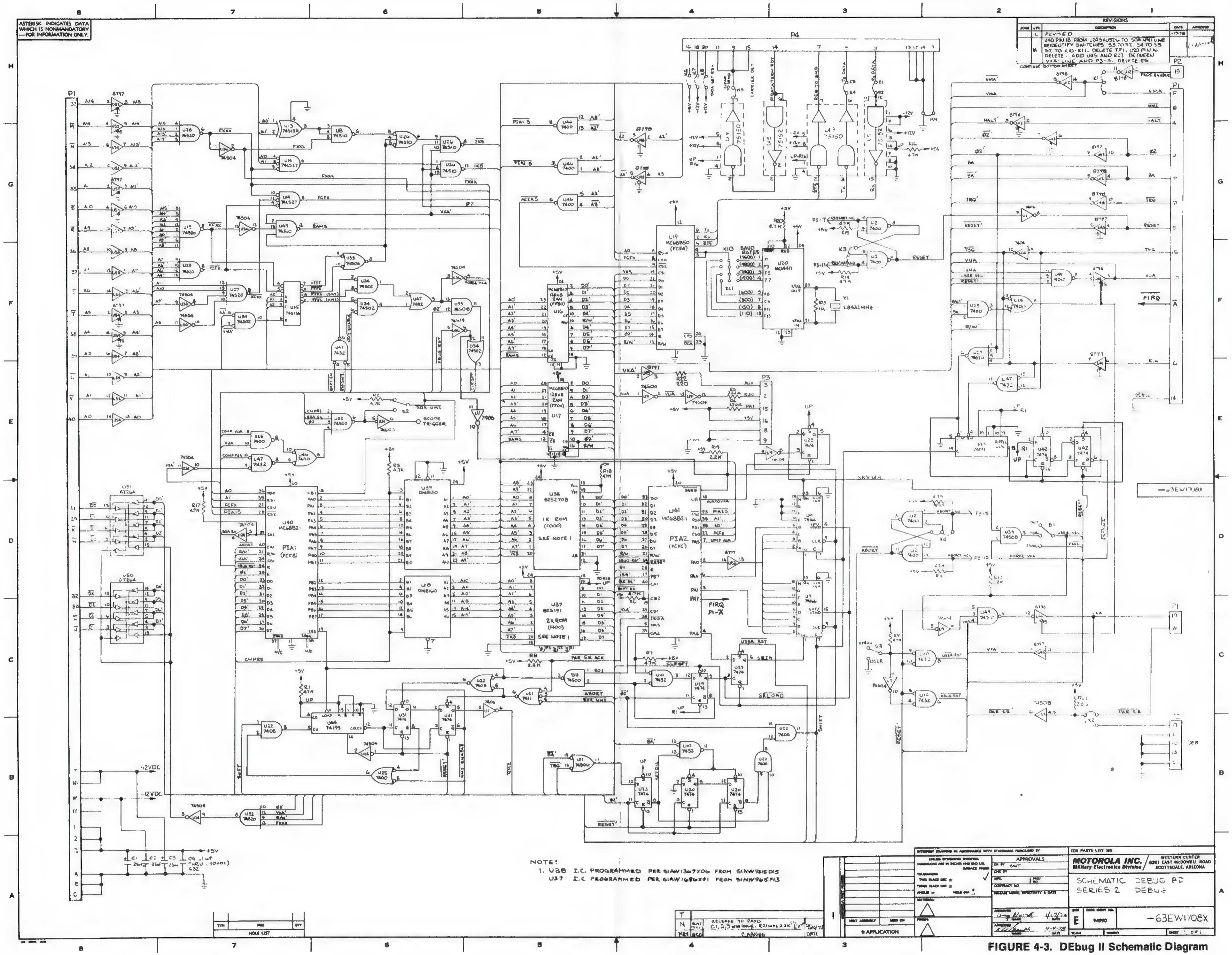
A User Reset or Executive Reset presets these registers to the required state. EXBUG-RESET causes both the shift register and the serial input flip-flop (refer to Figure 4-1) to be cleared so that only VXA pulses occur. USER-RESET causes the serial input flip-flop to be set so that only VUA pulses occur.

Three-State Logic, Shift Enable Logic: The Three-State Logic three-states the VUA and VXA drivers when either TSG occurs or the MPU is stopped due to a HALT on the system bus. The Shift Enable Logic outputs the SHIFT signal for the shift register and other devices on the module. This signal is normally $\overline{\phi 2}$ except when a BA or TSG occurs. The Shift Enable Logic does not output SHIFT pulses if BA or TSG is active, so that the MPU and the contents of the shift register and other devices stay synchronized with MPU instruction execution. Due to the relation of the shift clocks and the BA signal, SHIFT is disabled an extra two cycles whenever BA occurs. Since BA occurs in the first cycle of the instruction, this temporary lack of synchronization presents no problem.

Force VXA Logic, SWI Detect Logic: The Force VXA Logic generates two signals, CLEAR SHIFT (CLRSFT) and FORCE VXA. CLRSFT clears the shift register and the load logic in order to generate VXA. FORCE VXA is used by the VUA/VXA Control Logic to assure that both the NMI and SWI vectors come from the VXA map, when necessary. EXbug can then determine whether the User or EXbug should process the interrupt, depending on the cause and the flags set within EXbug. Control is returned to the VXA map when an NMI occurs only if the DEbug II Module caused the NMI; otherwise, the NMI is processed in the map in which it is running. SWI detection is more difficult. The execution of an SWI is detected by a counter which detects a Read, followed by seven Write cycles and another Read cycle. If this set of circumstances occurs, an SWI is being executed and ENABLE SWI (EN-SWI) occurs. Control returns to the VXA map only if EN-SWI occurs and BREAKPOINT ENABLE (BKPT-EN) has been set by EXbug in PIA2. While the SWI counter is clocked by SHIFT, TSG also is used to disable the shift clock. Since TSG could occur in the middle of the register, save sequence of an SWI, the SWI counter must be disabled immediately when it does occur. BA will never come up in the middle of an SWI, so the disabled SHIFT signal is adequate in this case.

TABLE 4-1. Detailed Timing of an Indexed Store to the User's Map

INSTRUCTION	CYCLE H	ADDRESS BUS	DATA BUS	VMA	VUA	VXA	SHIFT REG. LMN PRS	OUT (=S)	COMMENTS
EXBUG Set Up	—	See Text for Details		1/0	0	1/0	000000	0	Code Executed in VXA Map
CPX $FCFC	1	OP CODE Addr	OP CODE (BC)	1	0	1	000000	0	This instruction initiates loading of shift register
	2	OP CODE Addr +1	High Order Addr (FC)	1	0	1	000000		
	3	OP CODE Addr +2	Low Order Addr (FC)	1	0	1	000000	0 0	
	4	FCFC	Operand Data	1	0	1	000000	0	Data Dir Reg Accessed
	5	FCFD	Operand Data	1	0	1	000000	0	CA2 Occurs
STAA n,X	1	OP CODE Addr	OP CODE (A7)	1	0	1	010000	0	Shift Register
	2	OP CODE Addr +1	Offset	1	0	1	010000	0	Shift Circuit Enabled
	3	Index Reg.	Irrelevant	0	0	0	001000	0	First Shift Occurs
	4	Index Reg. + Offset (w/o carry)	Irrelevant	0	0	0	000100	0	
	5	Index Reg. + Offset	Irrelevant	0	0	0	000010	0	
	6	Index Reg. + Offset	Operand Data	1	1	0	000001	1	VUA Generated
EXBUG Code Continues	—	—	—	1/0	0	1/0	000000	0	Code Executed in VXA Map



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	L	REVISED	1-17-78	
	M	U40 PIN 18 FROM J24 5+U32-6 TO SOA NMI LINE REIDENTIFY SWITCHES S3 TO S2, S4 TO S5 S2 TO K10-K11. DELETE TP1. U20 PIN 16 DELETE. ADD U45 AND R22 BETWEEN VXA' LINE AND P3-3. DELETE E5		

CONTINUE BOTTOM SHEET

NOTE:
1. U38 I.C. PROGRAMMED PER 51AW1369X06 FROM 51NW961ED15
U37 I.C. PROGRAMMED PER 51AW1686X01 FROM 51NW965F13

REV	ECO	CHANGE	DATE
T			
N	8117	RELEASE TO PROD C1,2,3 was 100uf. R21 was 2.2K	9/20/78

NEXT ASSEMBLY | USED ON

★ APPLICATION

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND END USE SURFACE FINISH ✓
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TWO PLACE DEC ±
THREE PLACE DEC ±
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DR BY SWT
CHK BY
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CONTRACT NO
RELEASE AUTH. EFFECTIVITY & DATE
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APPROVED 4-4-78

FOR PARTS LIST SEE

MOTOROLA INC. Military Electronics Division / WESTERN CENTER 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA

SCHEMATIC DEBUG PD
SERIES 2 DEBUG

SIZE E | CODE IDENT NO. 94990 | -63EW1708X

SCALE | WEIGHT | SHEET 1 OF 1

FIGURE 4-3. DEbug II Schematic Diagram

CHAPTER 5
PARTS

5.1 INTRODUCTION

This chapter provides the parts list (Table 5-1) and parts location (Figure 5-1) for the DEbug II Module.

The parts list reflects the latest issue of hardware at the time of printing.

TABLE 5-1. DEbug II Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
	84DW6708X01	Printed Wiring Board, DEbug II Module	K
	55NW9403A10	Ejector, Circuit Card, with Roll Pin Attachment, 2 required	K
C1,C2,C3	23NW9618A33	Capacitor, Electrolytic, 25 μF at 16 Vdc, −10 + 50 Pct.	K
C4-C32	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 μF at 50 Vdc	K
K10,K11	28NW9802B88	Header, Double Row Post, 6-pin	K
P2	28NW9802C12	Header, Double Row Post, 20-pin	K
P3	28NW9802B04	Socket, DIL, 16-pin	K
R1,R2,R3 R6,R7,R9,R10,R11, R14–R18,R20	06SW-124A65	Resistor, Fixed, Carbon 4.7 kΩ, 5%, 1/4 W	K
R4,R5,R21,R22	06SW-124A33	Resistor, Fixed, Carbon, 220 Ω, 5%, 1/4 W	K
R8,R12,R19	06SW-124A57	Resistor, Fixed, Carbon, 2.2 kΩ, 5%, 1/4 W	K
R13	06SW-124B22	Resistor, Fixed, Carbon, 1.0 MΩ, 5%, 1/4 W	K
S1	40NW9801A81	Switch, Toggle, ON-OFF-ON, PC mount	K
S2,S3	40NW9801A32	Switch, Toggle, ON-OFF	K
U1	51NW9615A36	I.C. MC7406P	K
U2,U25,U46	51NW9615A32	I.C. MC7400P	K
U3,U4	51NW9615E57	I.C. SN7515OP	K
U5	51NW9615E79	I.C. SN75152N	K
U6,U7	51NW9615D28	I.C. 74166B	K
U8,U26,U49	51NW9615E34	I.C. 74S10A	K
U9,U24,U36	51NW9615C96	I.C. SN74S04N	K
U10,U47	51NW9615A79	I.C. SN7432N	K
U11	51NW9615C94	I.C. SN74S00N	K
U12,U48	51NW9615C36	I.C. 8T98	K
U13	51NW9615E78	I.C. SN74S135N	K
U14	51NW9615E77	I.C. SN74LS27N	K
U15	51NW9615D93	I.C. SN74S30N	K
U16,U17	51NW9615E80	I.C. MCM68B10P	K

TABLE 5-1. DEbug II Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
U18	51NW9615D95	I.C. DM8160N	K
U19	51NW9615D86	I.C. MC68B50	K
U20	51NW9615B54	I.C. MC14411P	K
U21	51NW9615C54	I.C. N7411A	K
U22	51NW9615A37	I.C. MC7408P	K
U23,U29,U30,U31,U42	51NW9615A47	I.C. SN7474N	K
U27,U28,U32	51NW9615D92	I.C. SN74S20N	K
U33	51NW9615C56	I.C. SN74S08N	K
U34	51NW9615D32	I.C. SN74S01N	K
U35	51NW9615C34	I.C. SN74S138N	K
U37	51AW1671X02	I.C. Programmed, EXbug 2.1	M
U37	51NW9615F13	I.C. Alterable, N82S191-I	K
U38	51BW1630X03	I.C. EXbug I/O	M
U38	51NW9615F17	I.C. N82S181F	M
U38	51AW1369X10	I.C. Programmed (Alternate)	M
U38	51NW9615D15	I.C. Alterable, 82S2708 (Alternate)	M
U39	51NW9615D94	I.C. DM8130	K
U40,U41	51NW9615D85	I.C. MC68B21P	K
U43	51NW9615D88	I.C. SN74191N	K
U44	51NW9615A65	I.C. MC74193P	K
U45,U52,U53,U54	51NW9615B71	I.C. 8T97	K
U50,U51	51NW9615F19	I.C. 8T26A	K
Y1	48BW1357X01	Crystal Oscillator 1.8432 MHz 3 lead	K
	29NW9805A44	Terminal, Stud, Turret (Use at Scope Trigger)	K
	28NW9802B08	Socket, DIL, 24-pin (Use at U37,U38)	K
	29NW9805A91	Jumper, 2-position (Use at K10,K11)	K

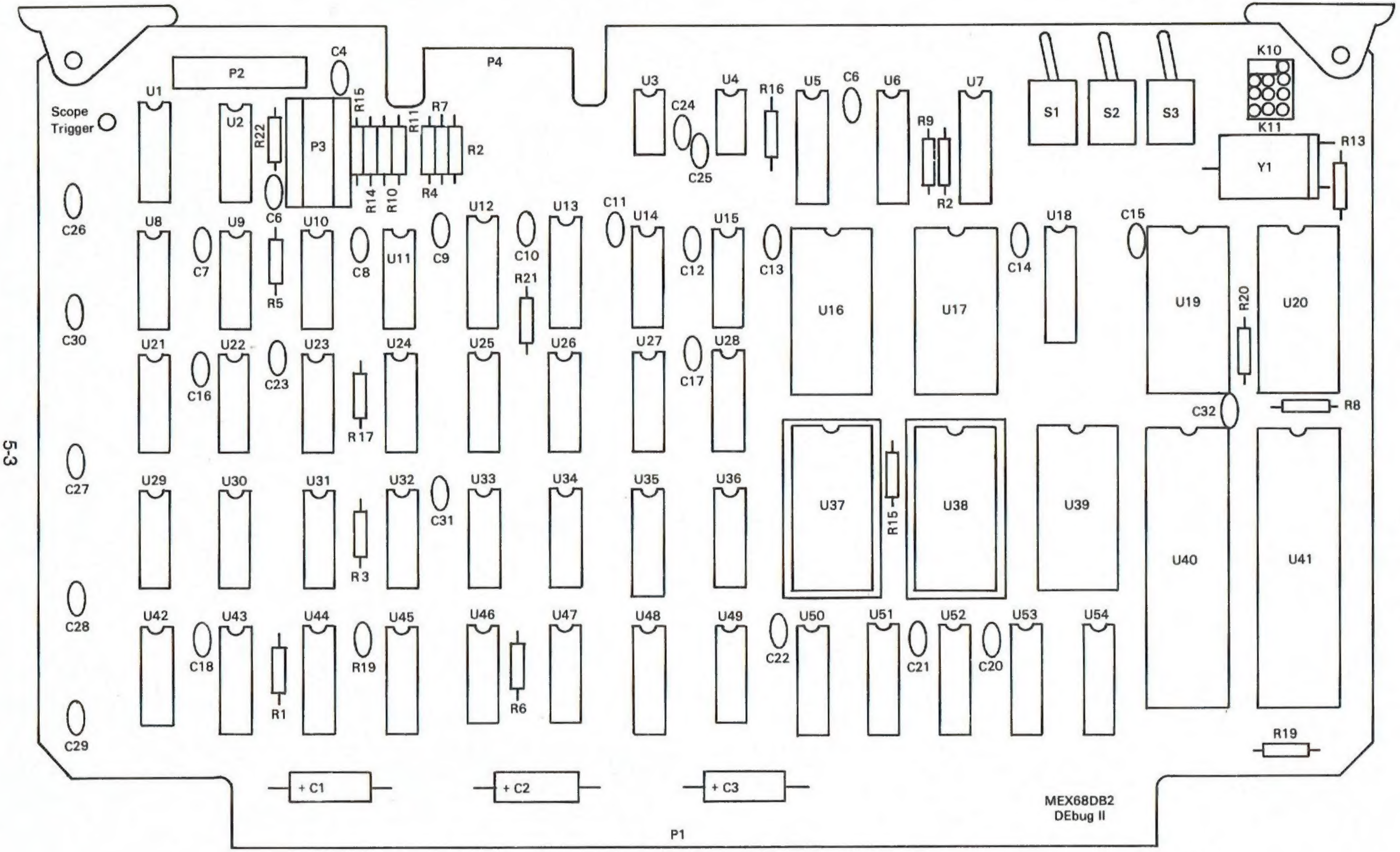

FIGURE 5-1. DEbug II Module, Parts Location

MOTOROLA INC.
Integrated Circuits Division

Microsystems • P.O. Box 20912 • Phoenix, Arizona 85036

12059-1 PRINTED IN USA 4/79 IMPERIAL LITH